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MS-7562 UATX Version: 0A

CPU: Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Yorkfield processors in LGA775 Package.

System Chipset:

Intel Eaglelake - Q45 (North Bridge)
Intel ICH10DO (South Bridge)

On Board Device:

CLOCK Gen -- ICS9LPRS113A
LPC Super I/O -- Fintek F71882F
LAN -- LAN Intel 82567
JMB368 IDEX1
JMB381-1394
HD Audio Codec -- ALC888
PCIE to DVI Interface
PCIE to Display port Interface

Main Memory:

Dual-channel DDR-II * 4

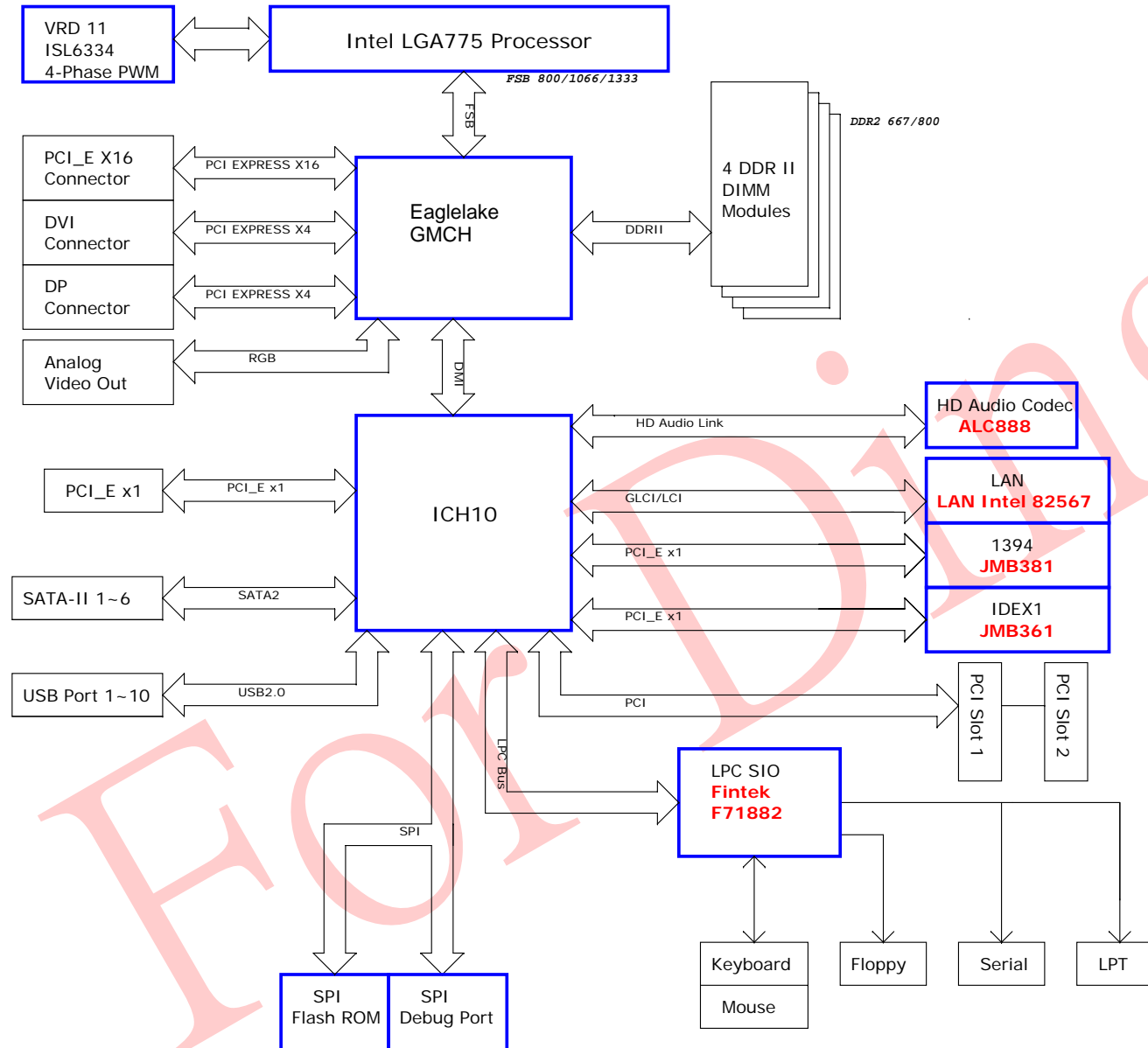
Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X4 share to DVI
PCI EXPRESS X4 share to Display port
PCI EXPRESS X1 SLOT * 1
PCI SLOT * 2

PWM: ISL6334 4Phase

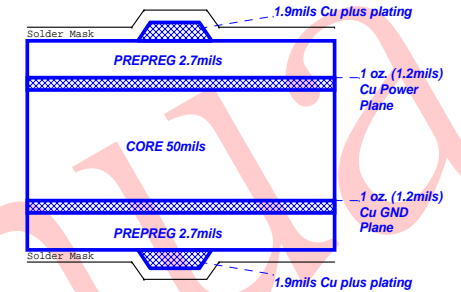
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Block Diagram



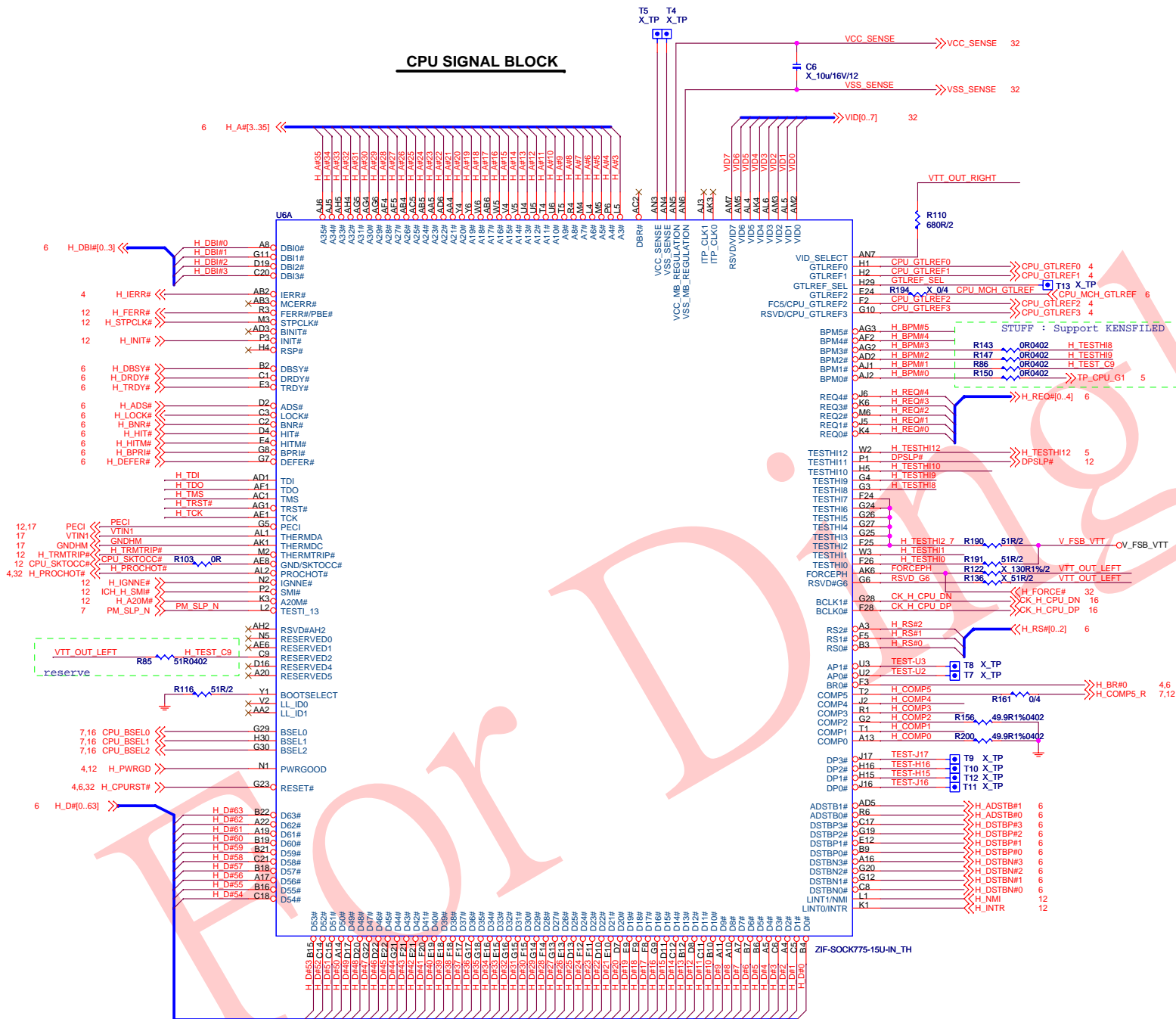
Board Stack-up

(1080 Prepreg Considerations)

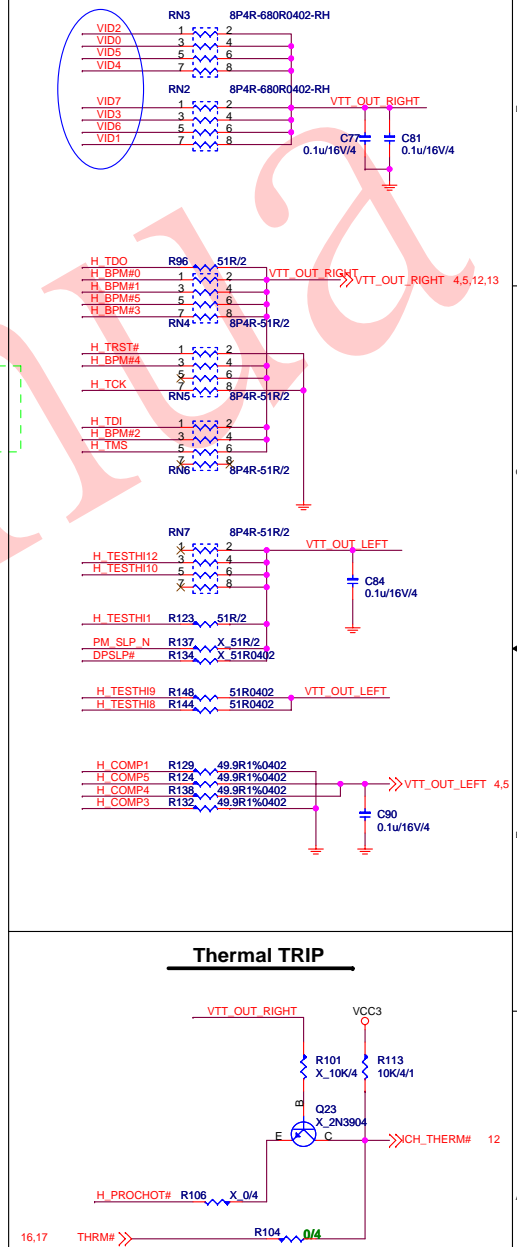


Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15

CPU SIGNAL BLOCK



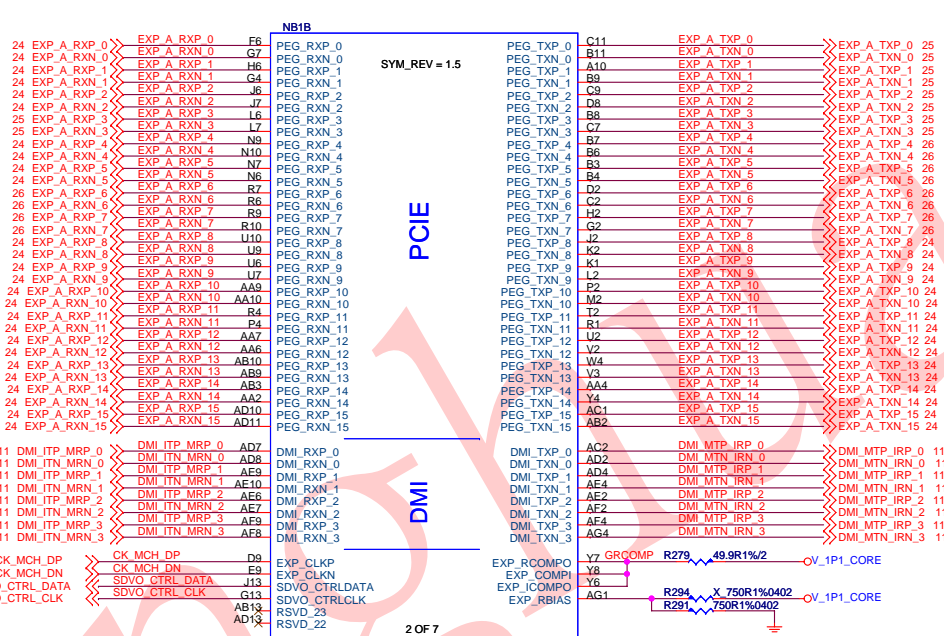
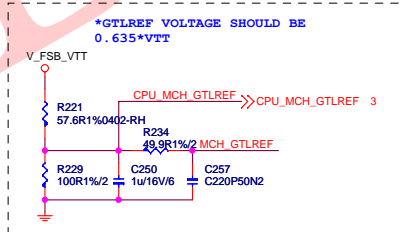
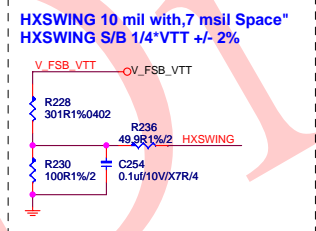
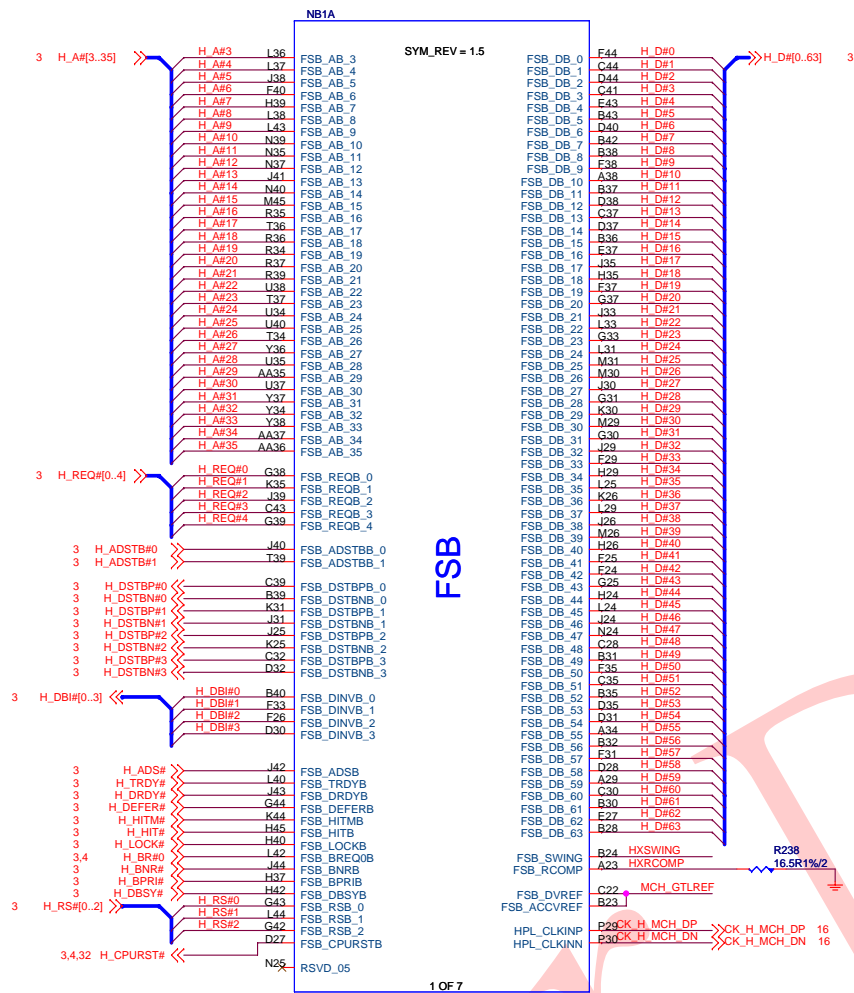
PULL HIGH PULL DOWN

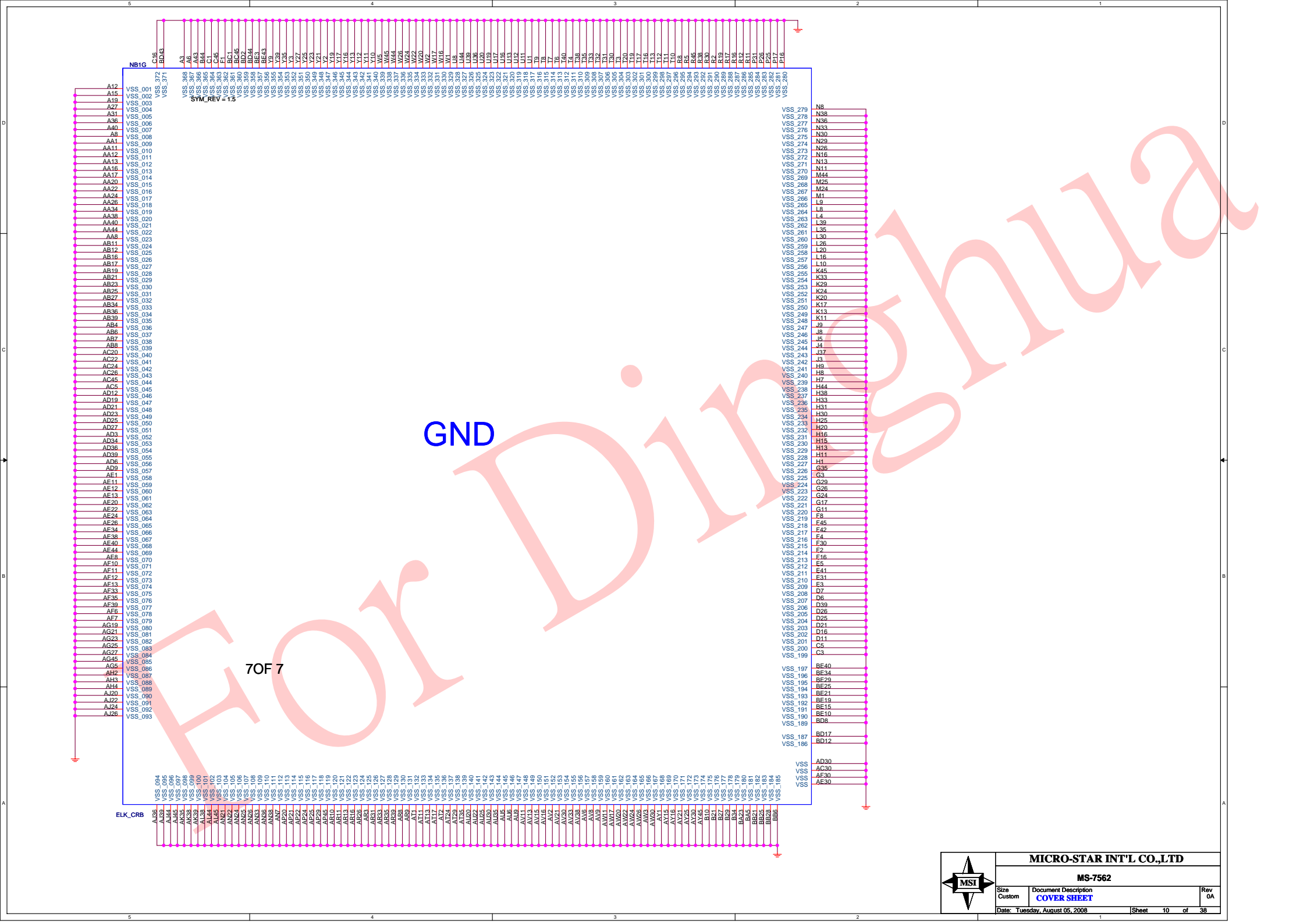


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GND

70F7

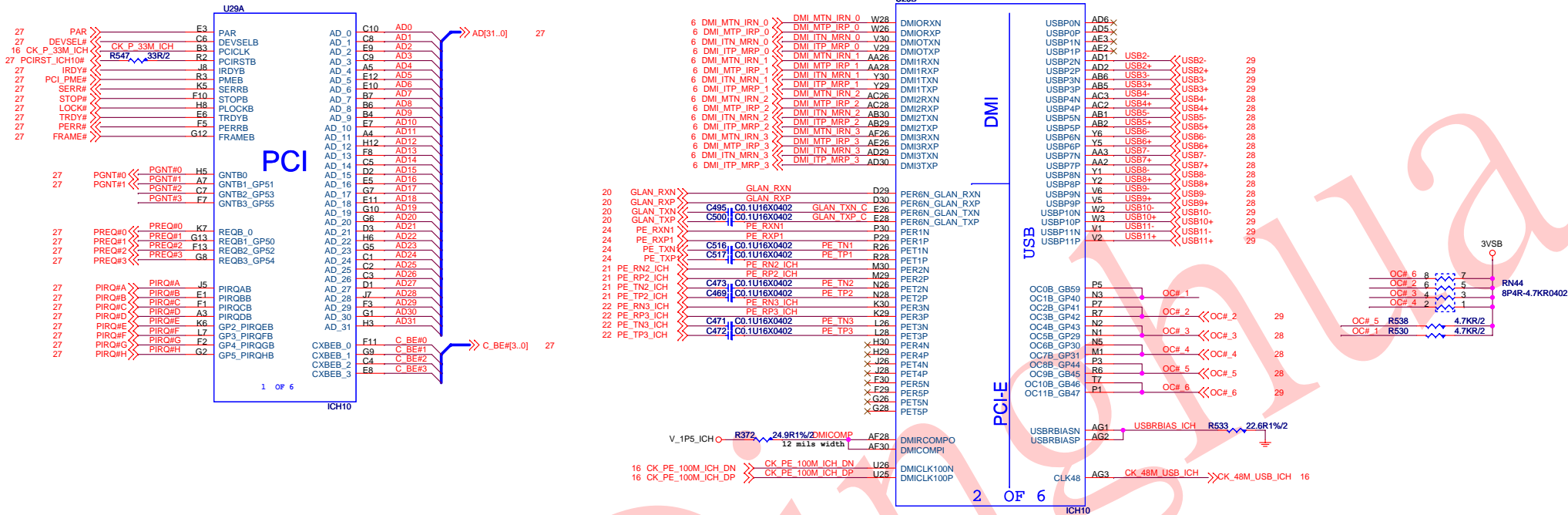


MICRO-STAR INT'L CO.,LTD

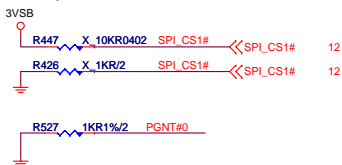
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SB STRAPPING RESISTOR



PGNT#[3:0] Internal Pull-up

SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

HDA_SDOUT/HDA_SYNC strap PCI_E port configuration bit[1:0]. Internal weak pull down.
00:1X/1X/1X 11:0X/0X/4X

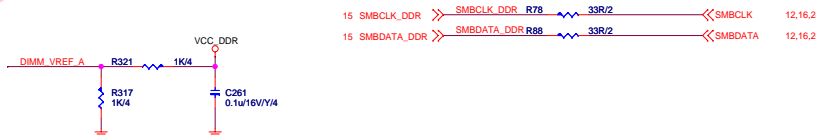
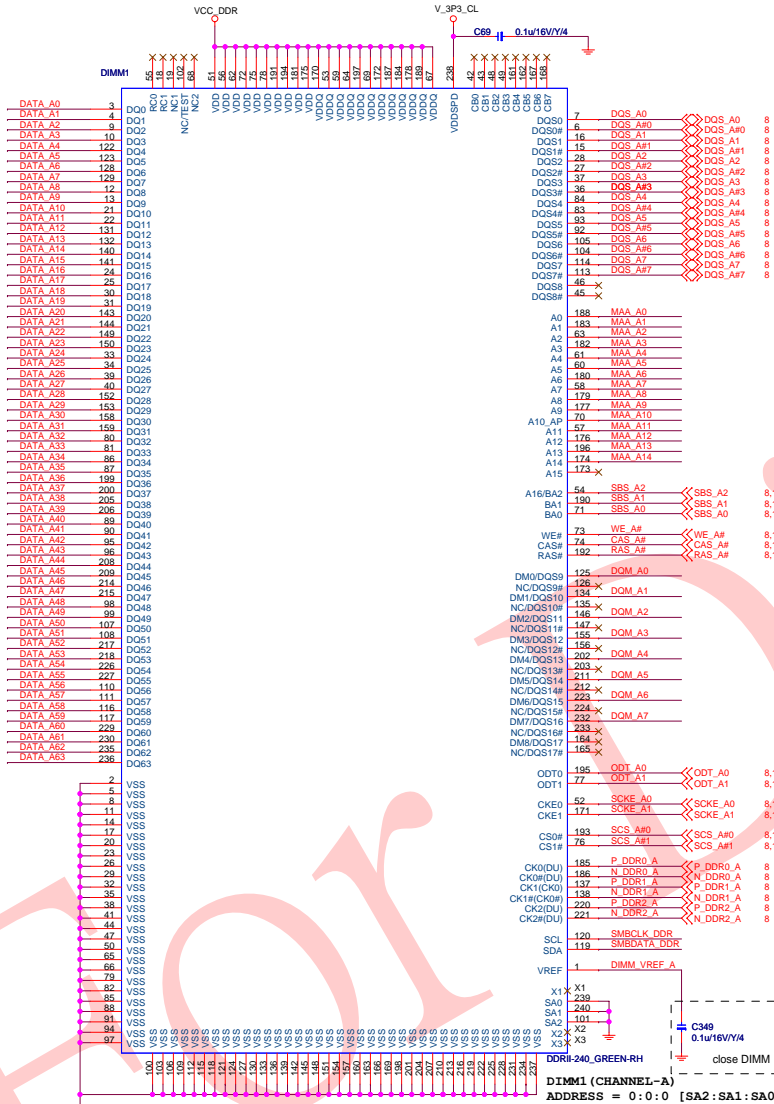
BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	X
PCI	1	0

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Size Custom	Document Description ICH10 - PCI, DMI, USB, PCIE & Slots	Rev 0A
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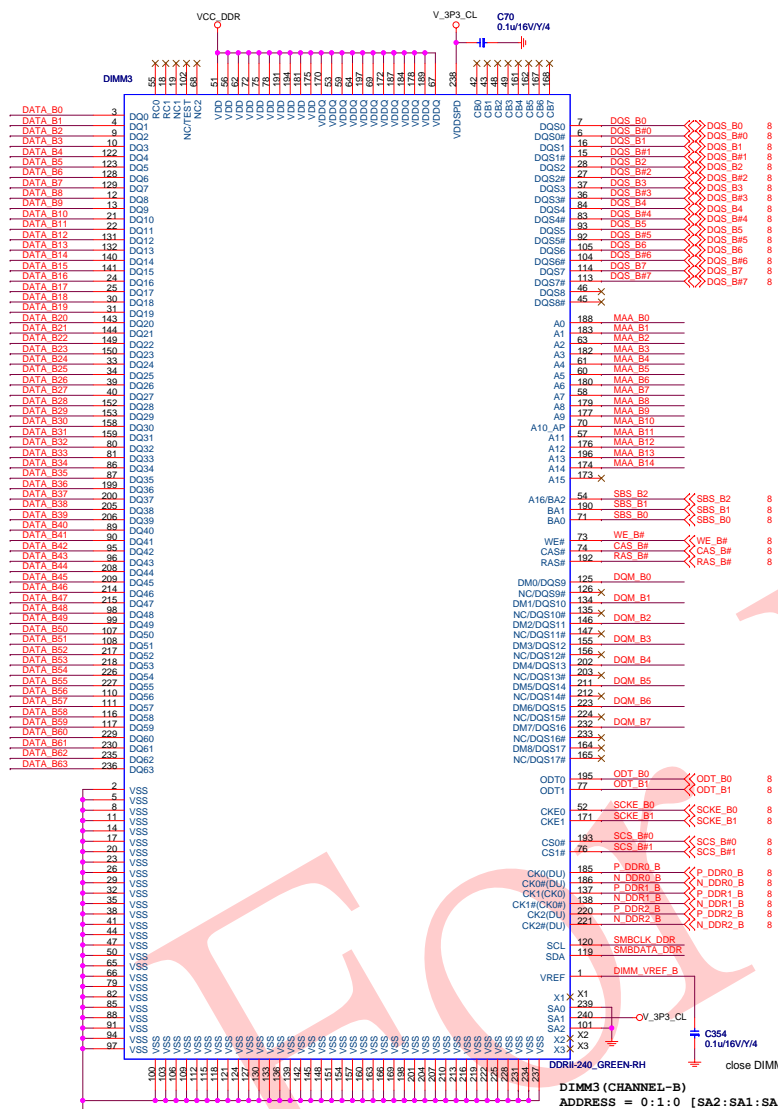
DDR2 DIMM_A1

DDR2 DIMM_A2

8 DQM_A[0..7] >> DQM_A[0..7]
8.15 MAA_A[0..14] >> MAA_A[0..14]
8 DATA_A[0..63] >> DATA_A[0..63]



DDRII DIMM_B1

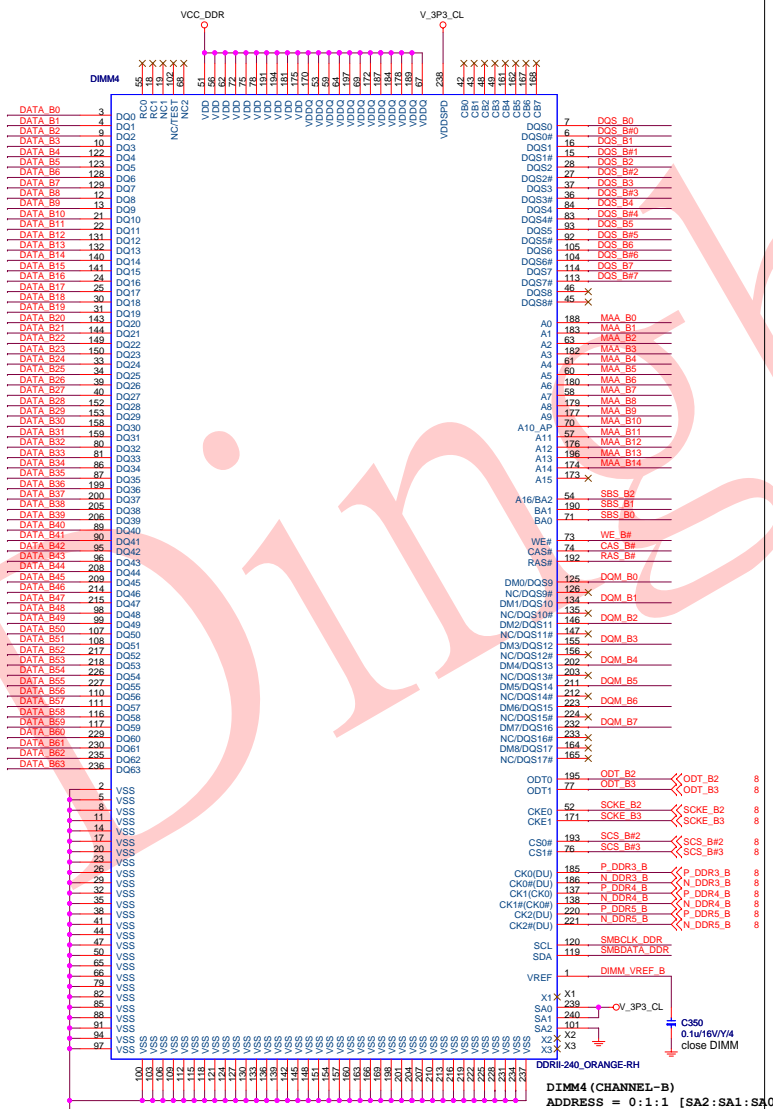


Place close to DIMM3

Place close to DIMM3 with DIMM4



DDRII DIMM_B2



DIMM4 (CHANNEL-B)

ADDRESS = 0:1:1 [SA2:SA1:SA0]



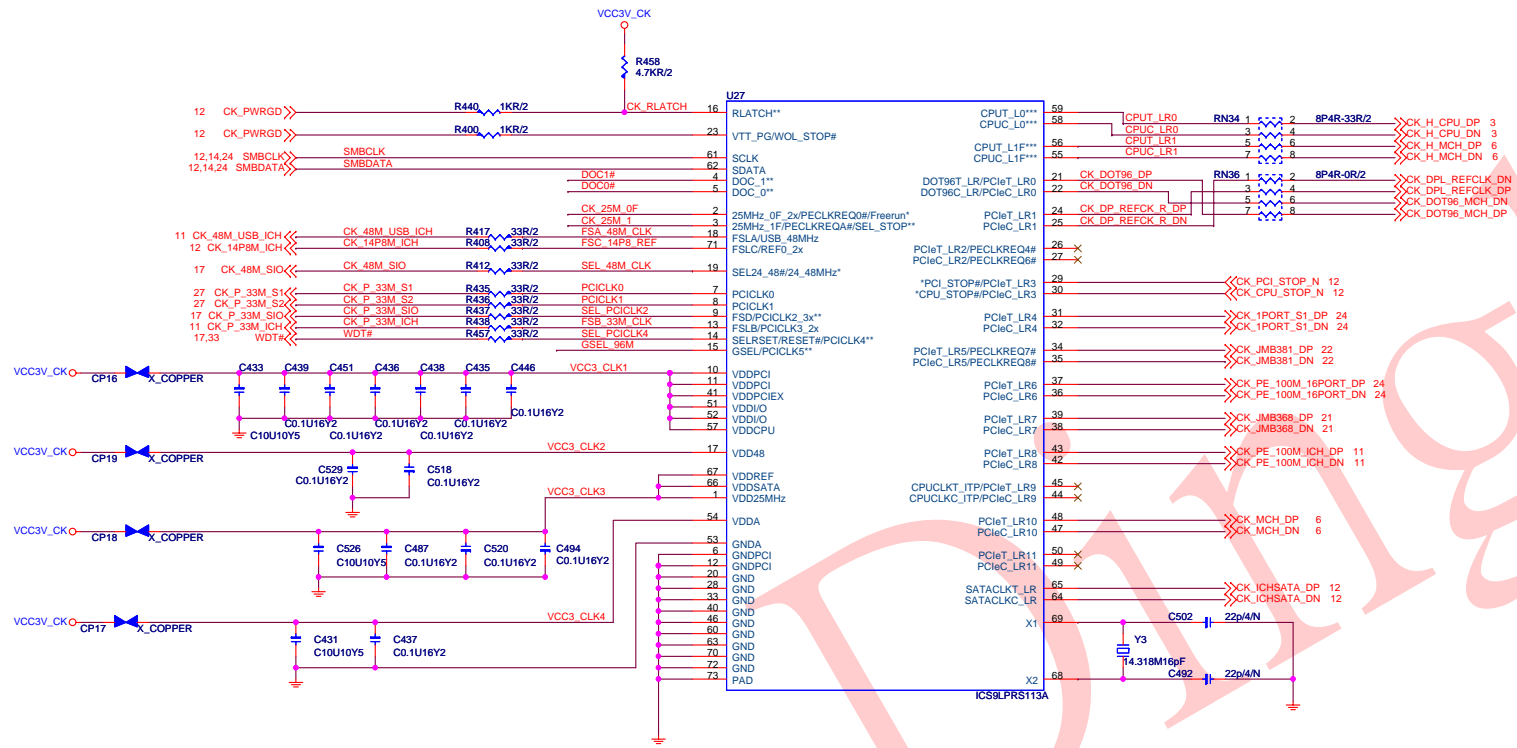
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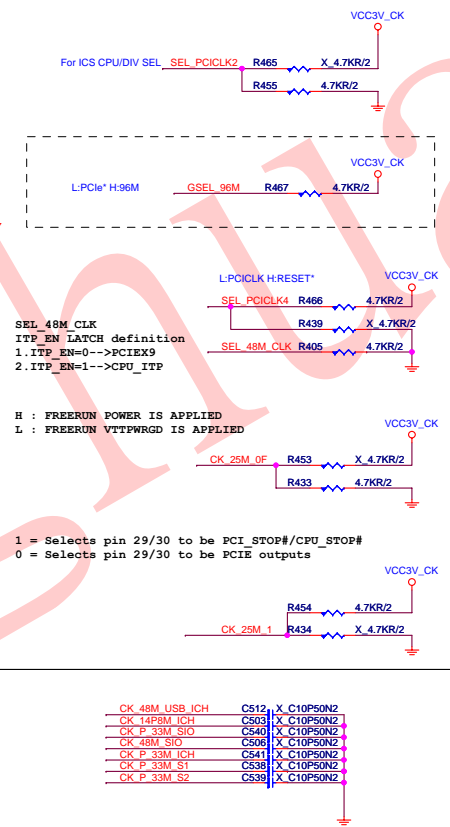
Size	Document Description	Re
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C	DDR3 Chanel-A / Chanel-B	
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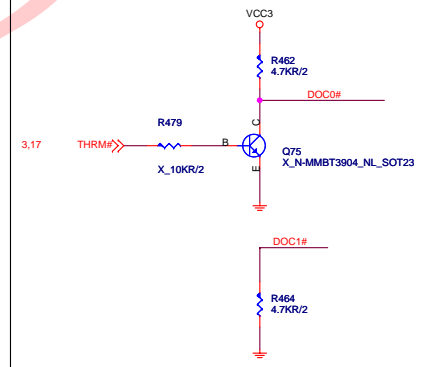
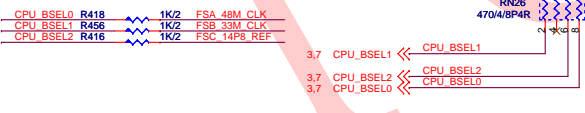
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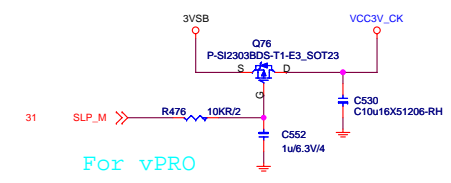
CLOCK GEN STRAPING



BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	266 MHz (1066)
1 0 0	333 MHz (1333)
0 1 0	200 MHz (800)
1 1 0	400 MHz (1600)



AMT POWER

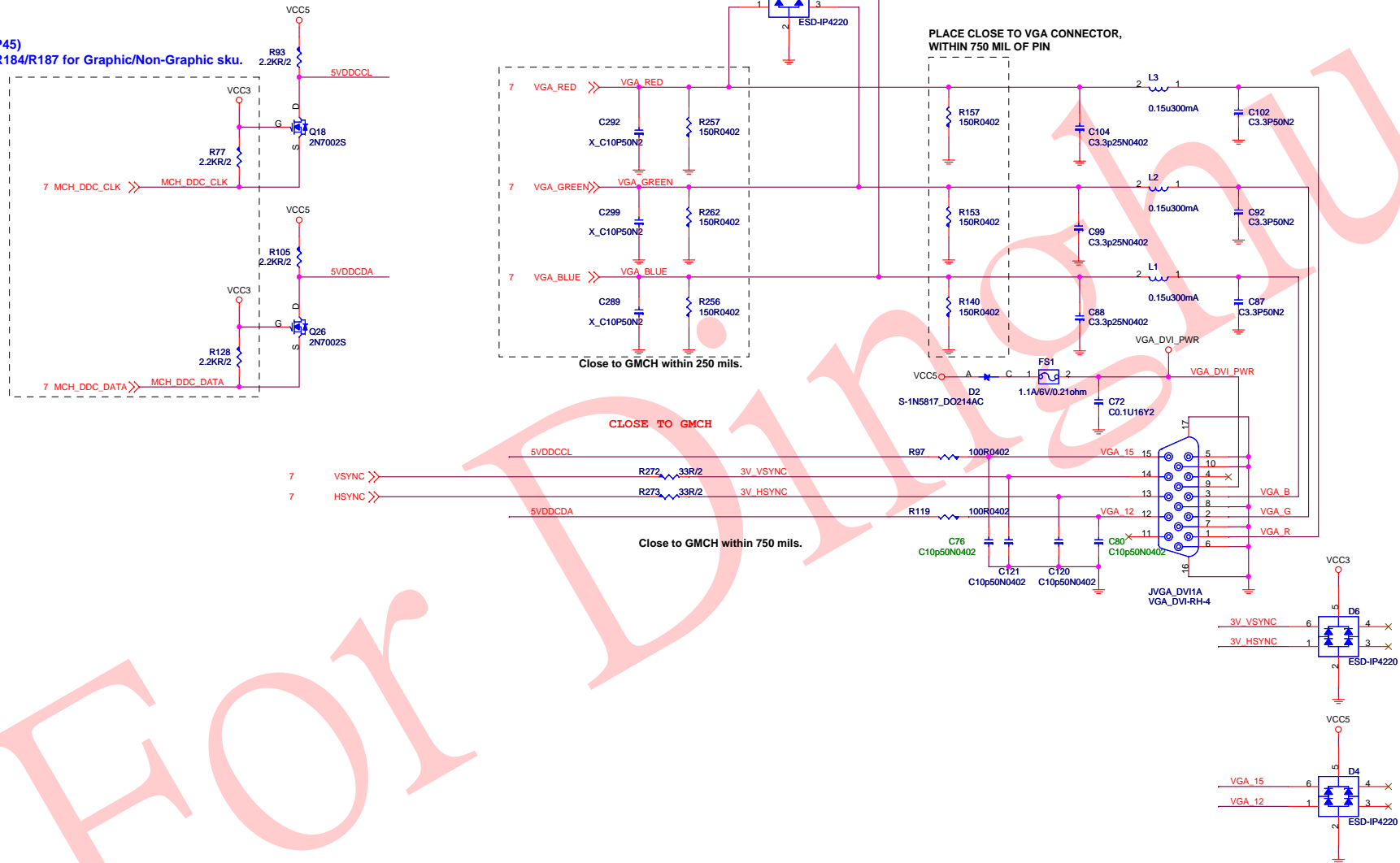


For vPRO

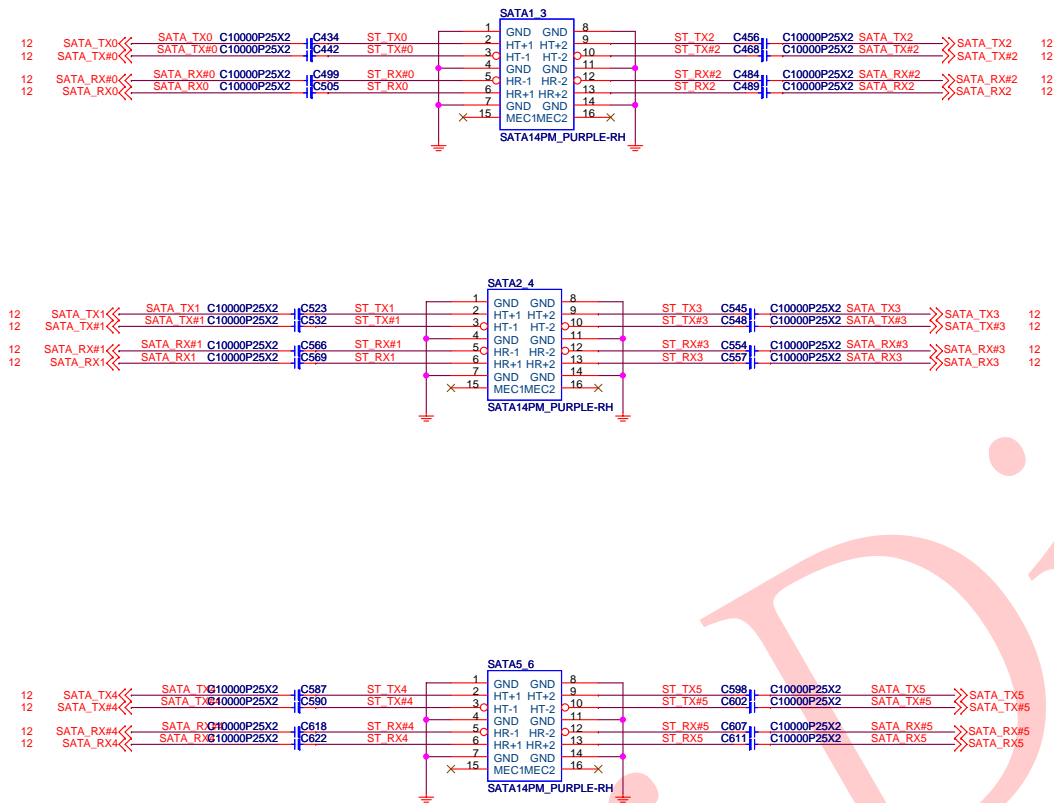


Video Connector

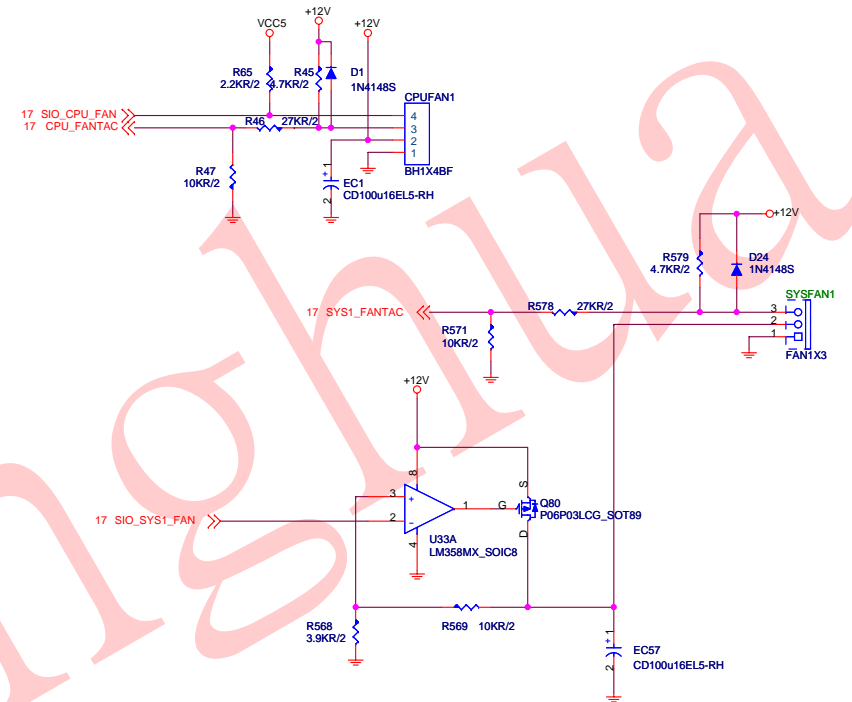
FOR V10 (NB:P45)
Always Stuff R184/R187 for Graphic/Non-Graphic sku.




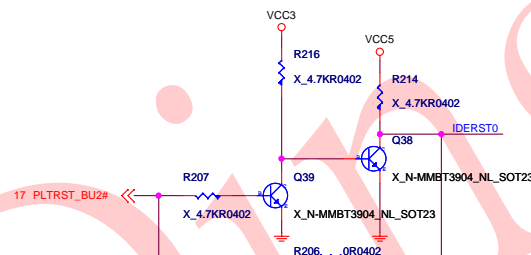
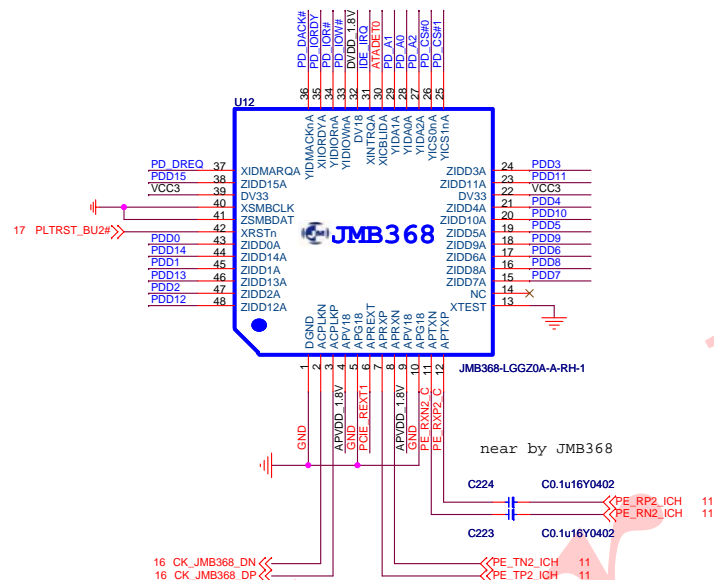
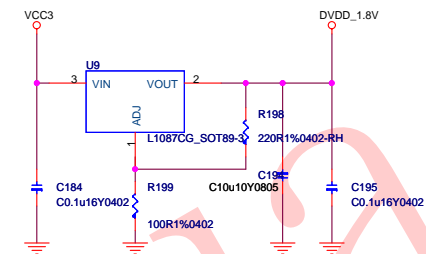
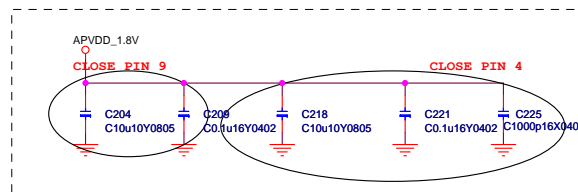
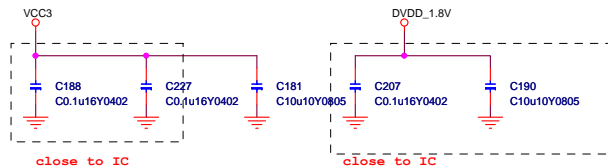
SATA 1- 6 PORT



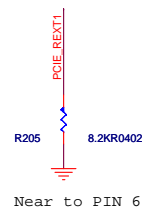
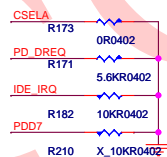
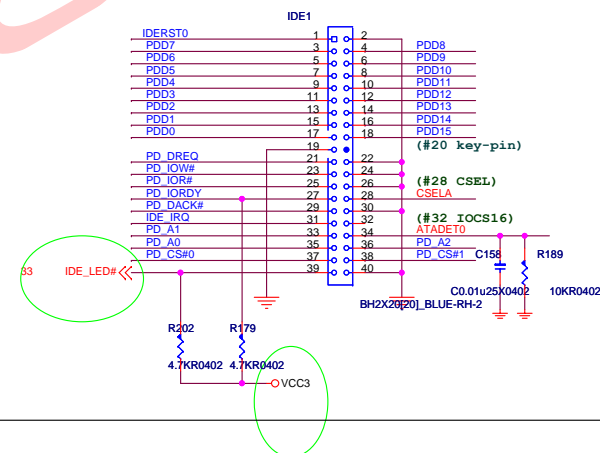
FAN-COUNT CIRCUIT

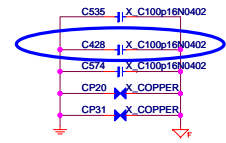
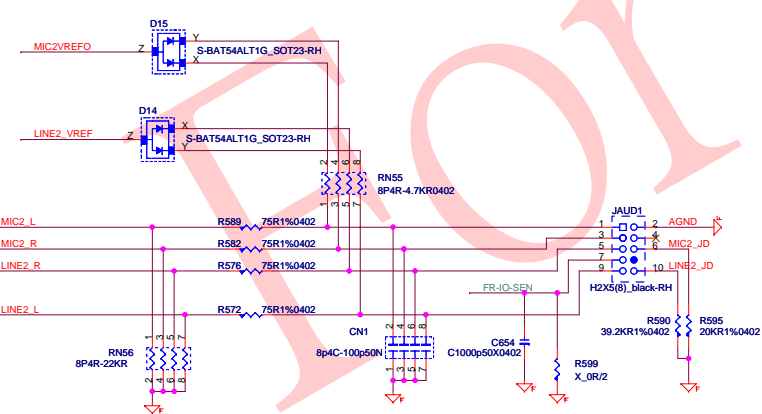
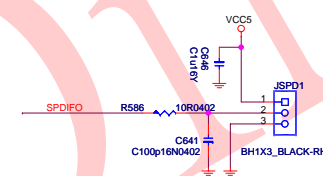
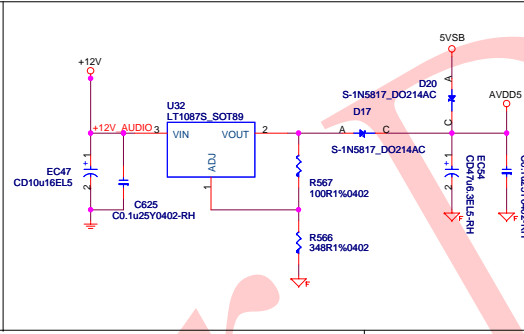
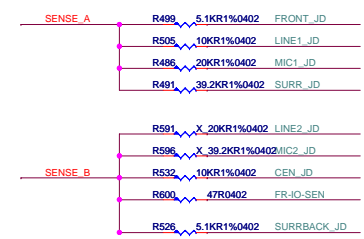
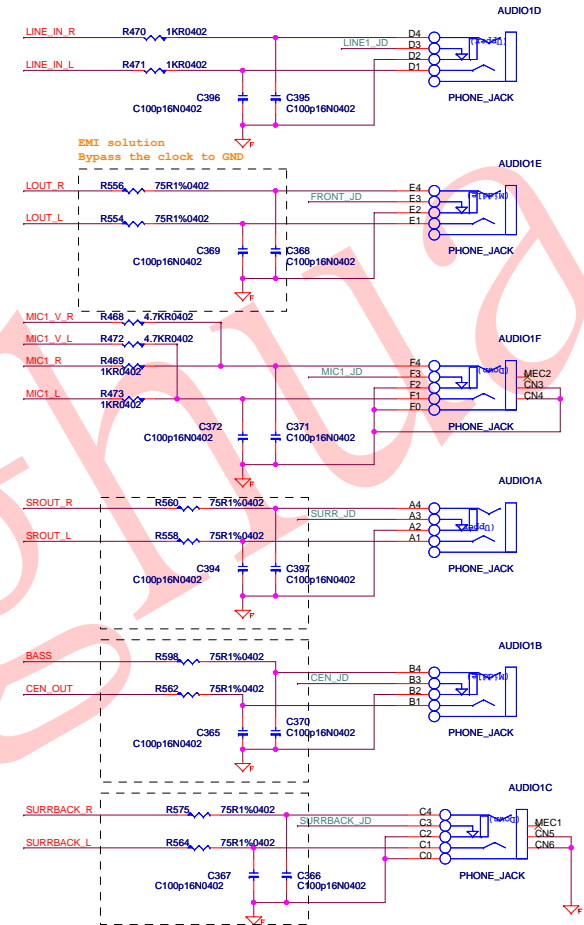
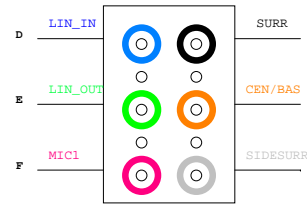
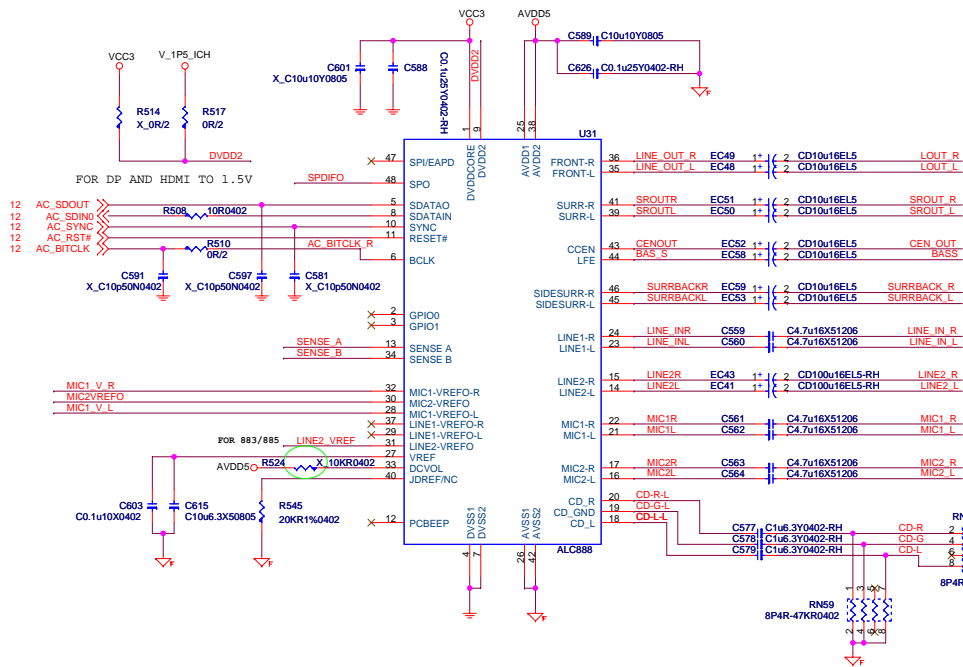


			
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Custom	SATA & e-SATA Ports and Fan Control	0A	
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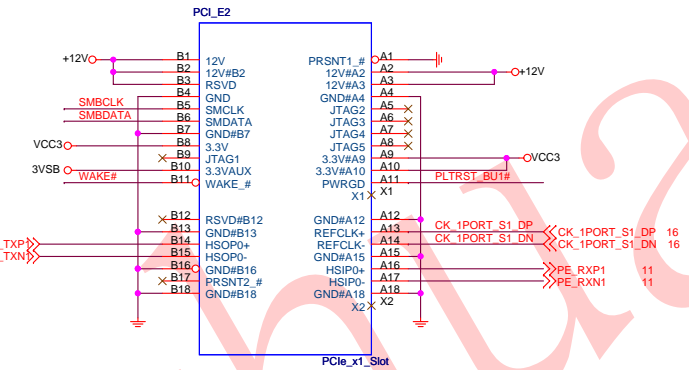


IDE Connector





PCI Express X1 Slot



SLOT-PCI164P-2PITCH-RH-7



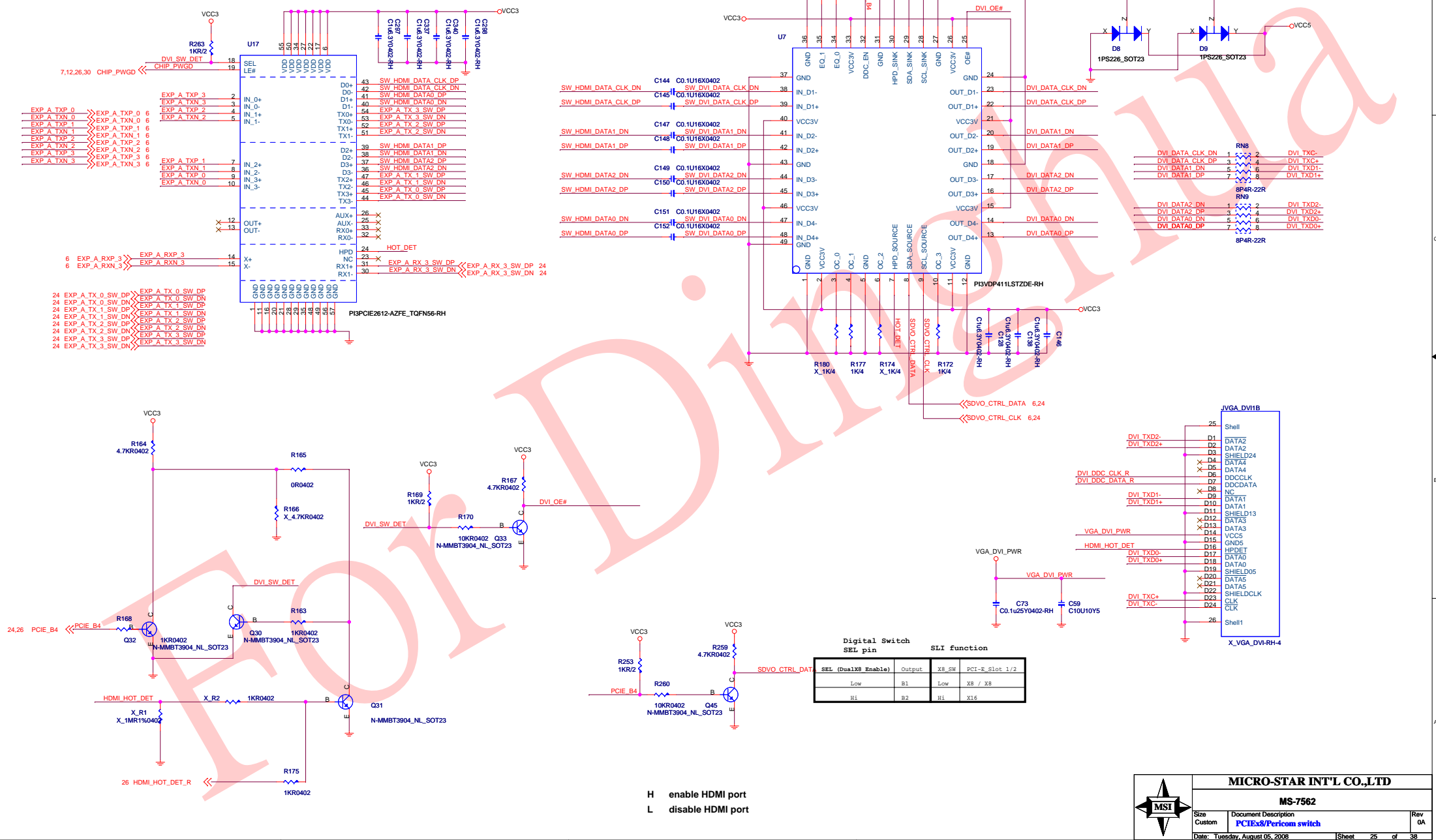
MS-7562

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0A

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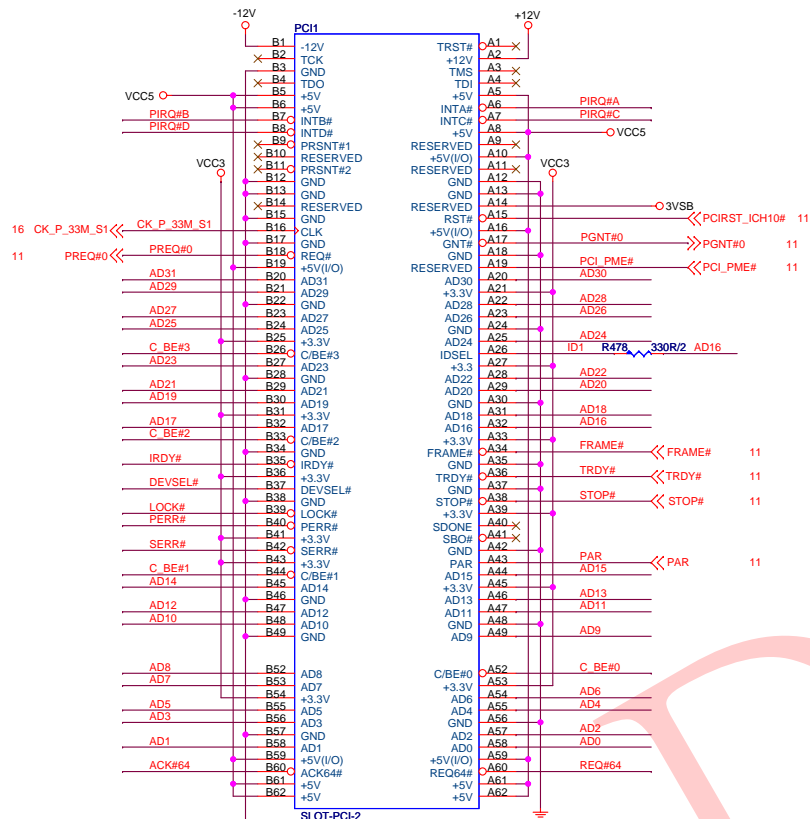
DVI/HDMI TRANSFER

(Share PCI_E x4 form PCI_E x16 Slots)



H enable HDMI port
L disable HDMI port

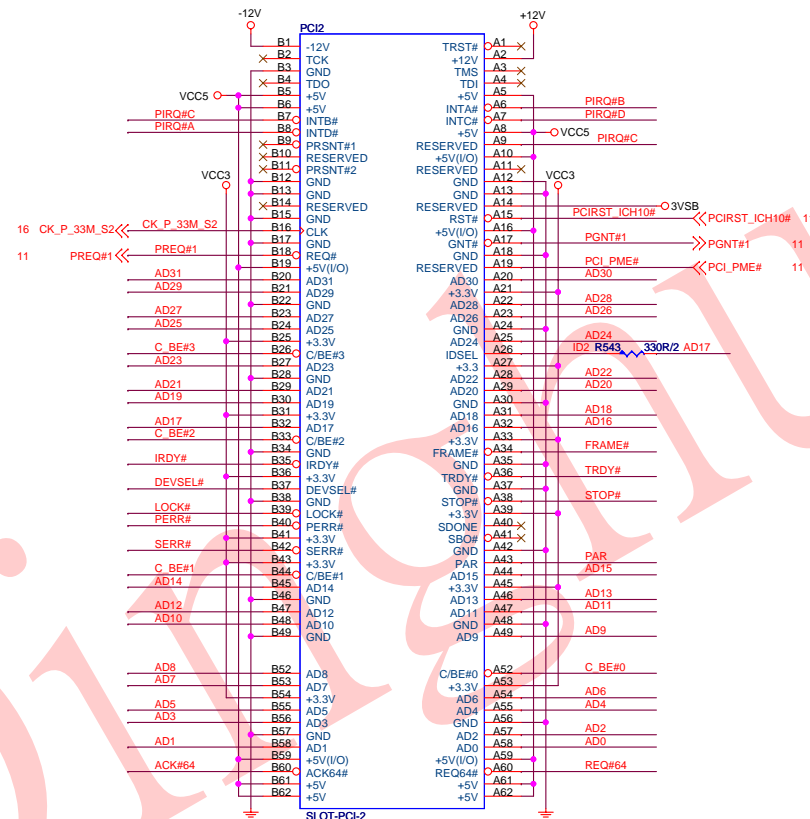
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

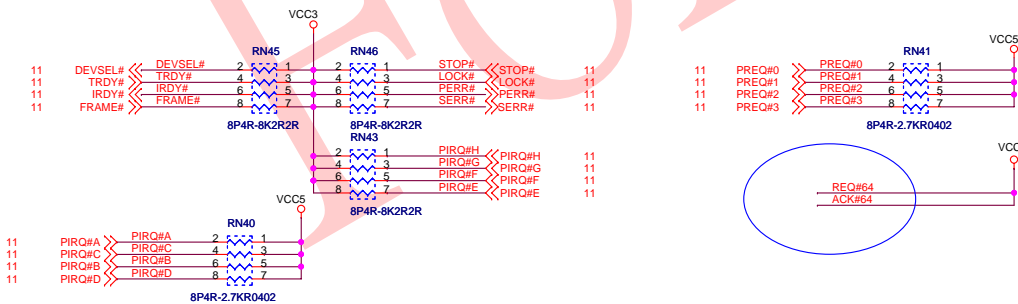
11 AD[31..0] << AD[31..0]
11 C_BE#[3..0] << C_BE#[3..0]

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

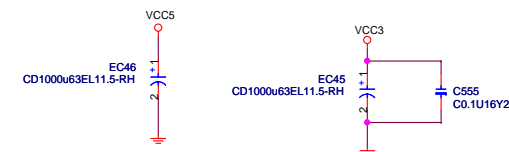


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

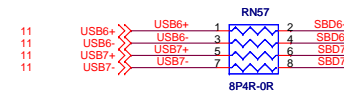
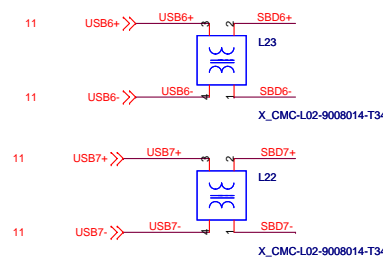
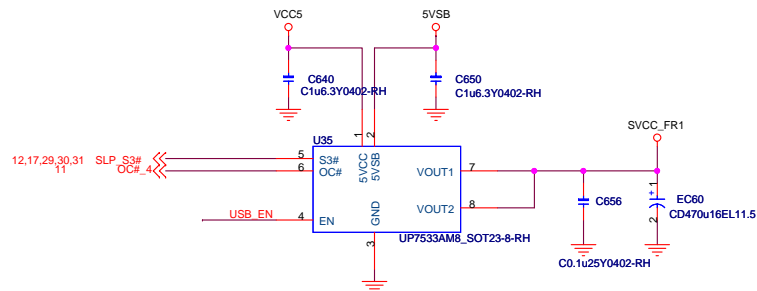


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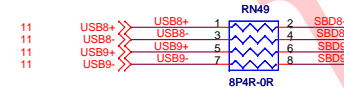
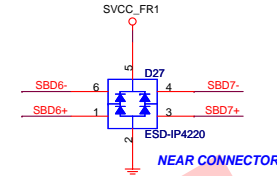
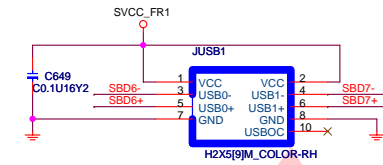
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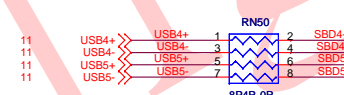
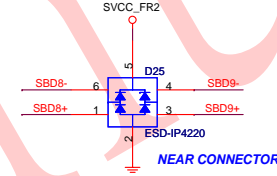
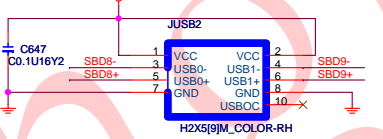
Front USB Connector



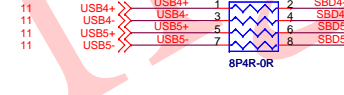
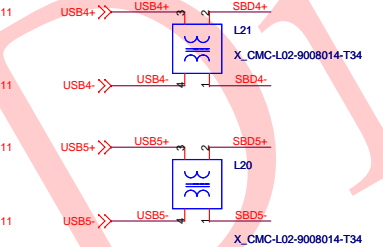
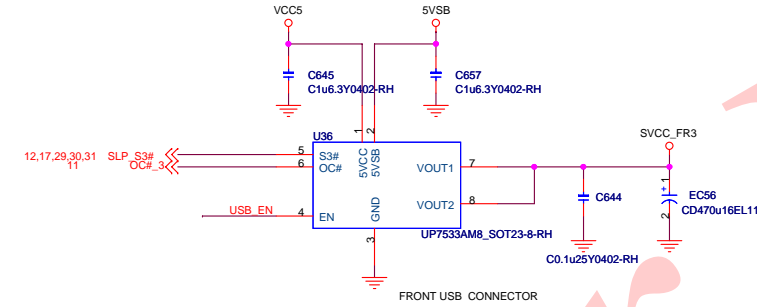
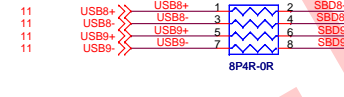
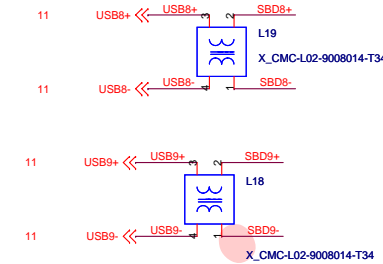
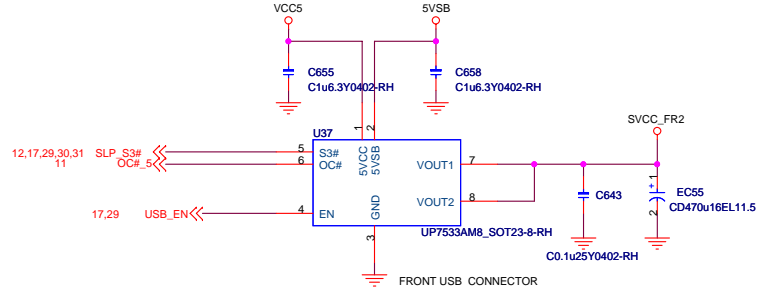
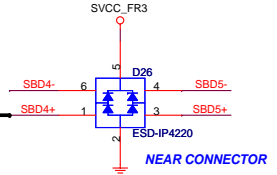
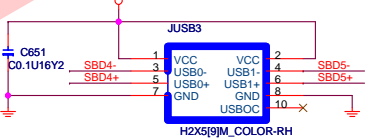
FRONT USB PORT2,3



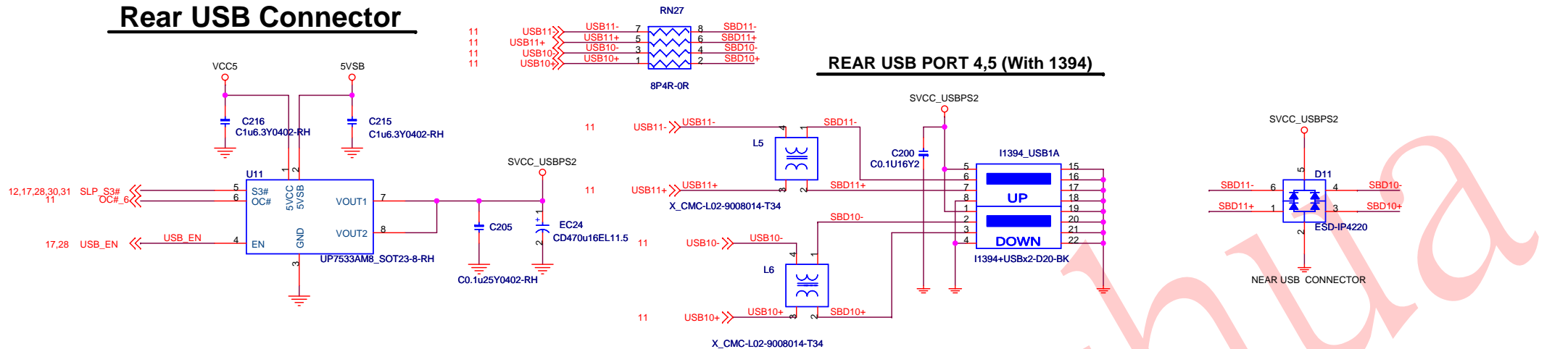
FRONT USB PORT 8,9



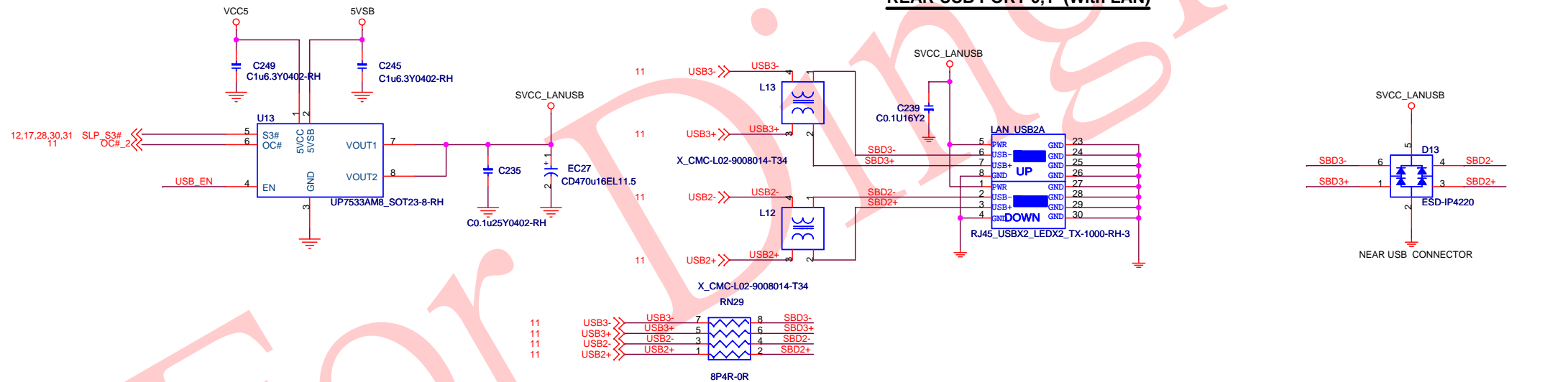
FRONT USB PORT 6,7



Rear USB Connector



REAR USB PORT 0,1 (With LAN)

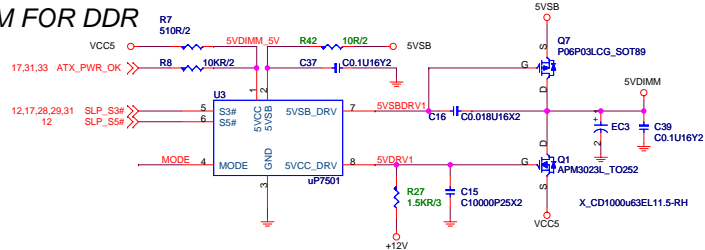


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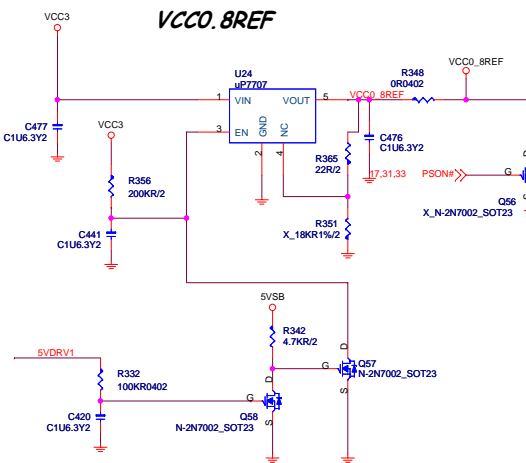
5VDIMM FOR DDR



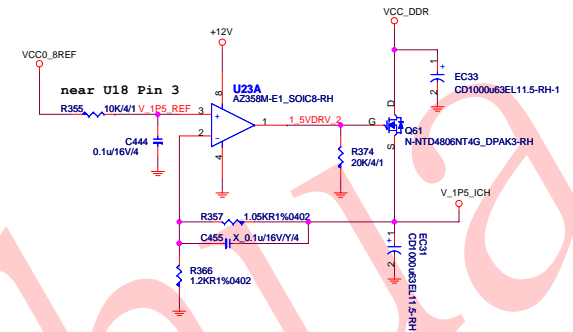
GPIO, Default=L
H: Support S0/S3/S4/S5
L: Support S0/S3

S5#	S3#	DUAL_CTRL	5VDUAL	REMARKS
1	1	X	5VCC	S0/S1/S2(Active)
1	0	X	5VSB	S3
0	X	1	5VSB	S4/S5
0	X	0	Showdown	S4/S5

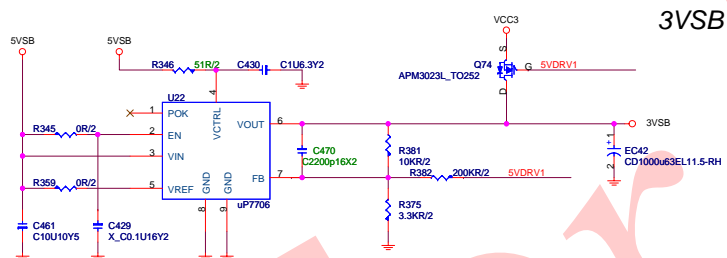
VCC0.8REF



SB 1.5V 2.4A



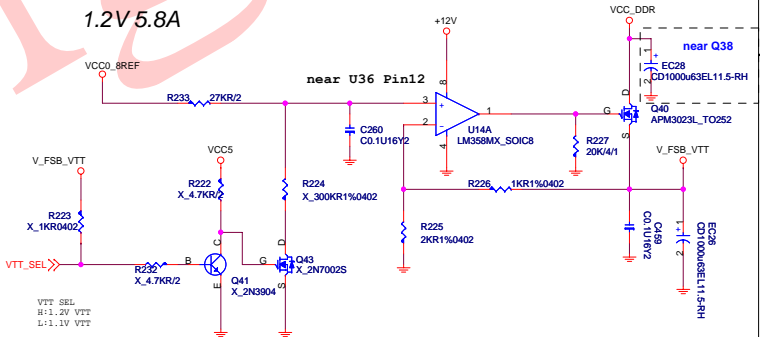
3VSB



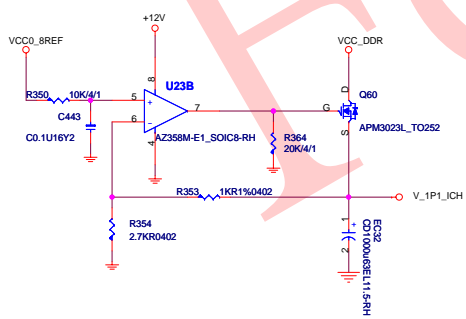
For power 700W solution
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

	S0	S3	S4	S5
DUAL_CTRL	X	X	0 1 1	0 1 1
5VSBDRV1	1	0	1 0 0	1 0 0
5VDRV1	1	0	0 0 0	0 0 0
5VSBDRV2	X	0	1 0 0	1 0 0
USB_MODE	X	1	X 1 0	X 1 0
5VDIMM	Y	Y	N Y Y	N Y Y
USB power	Y	Y	N Y N	N Y N

1.2V 5.8A

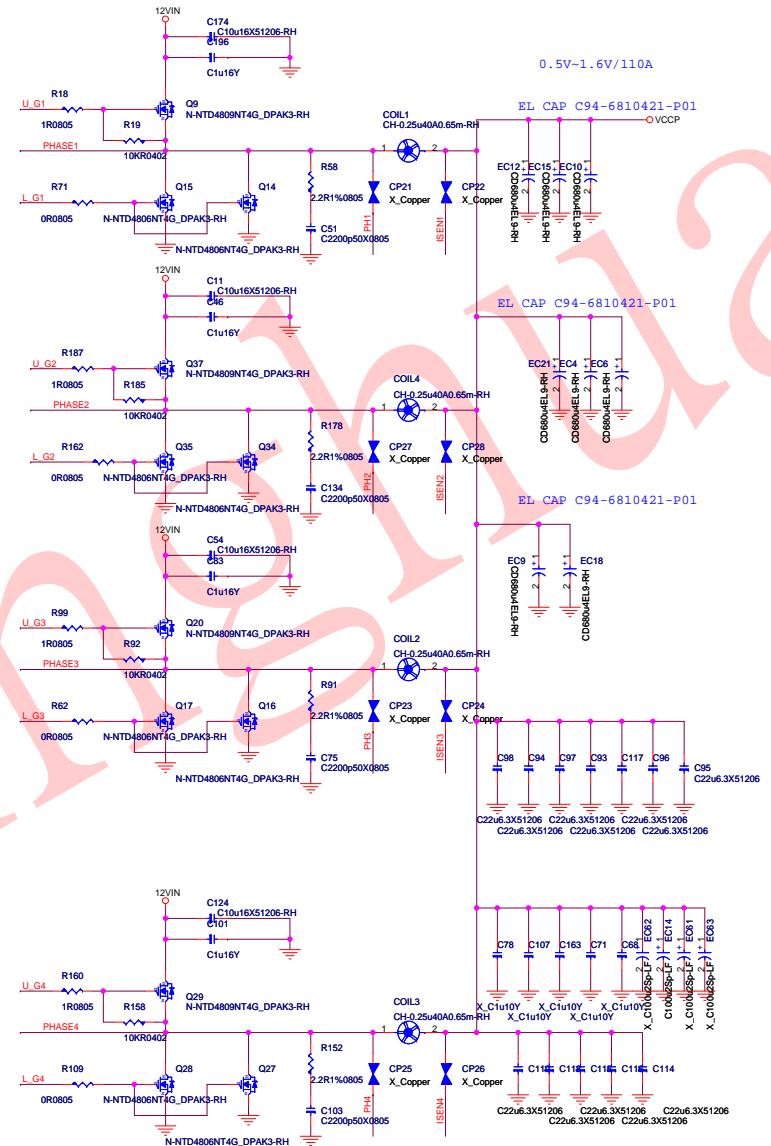
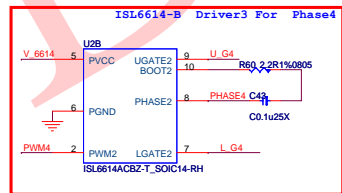
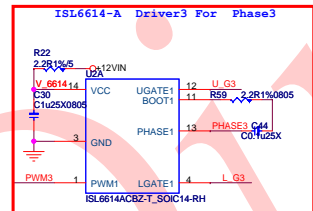
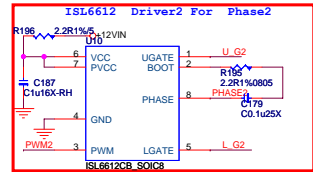
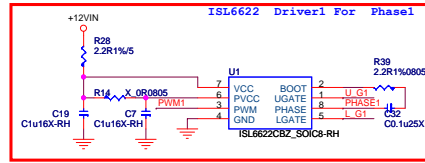
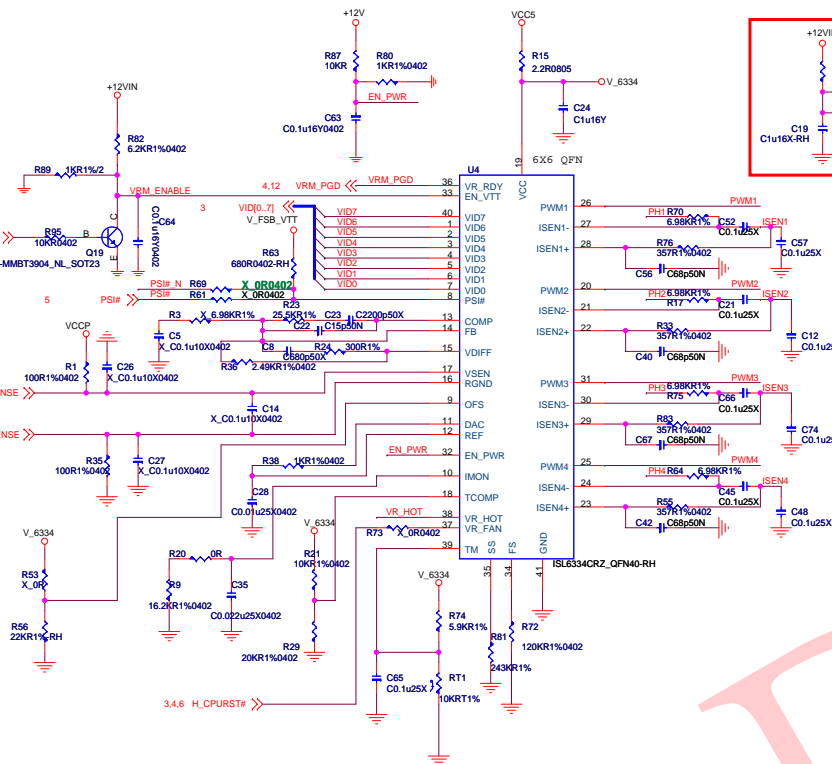


SB 1.1V 1.16A

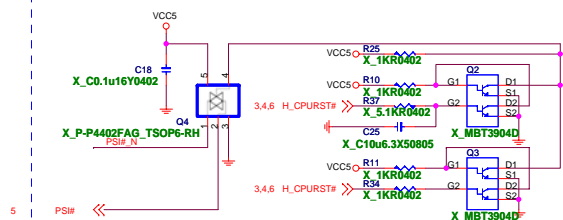


FIELD	OEM/ODM	CHANNEL
ADD	R26, R16, R30, R40, Q5	R6, R31
REMOVE	R6, R31	R26, R16, R30, R40, Q5
CHANGE	R5 => C5=0.1uF	C5=> R5=51Kohm

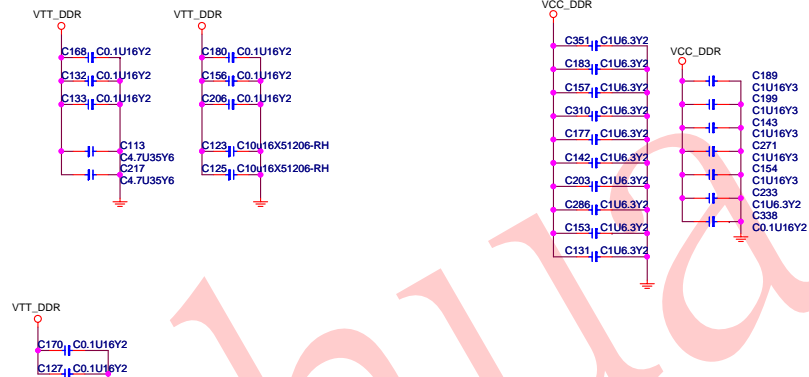
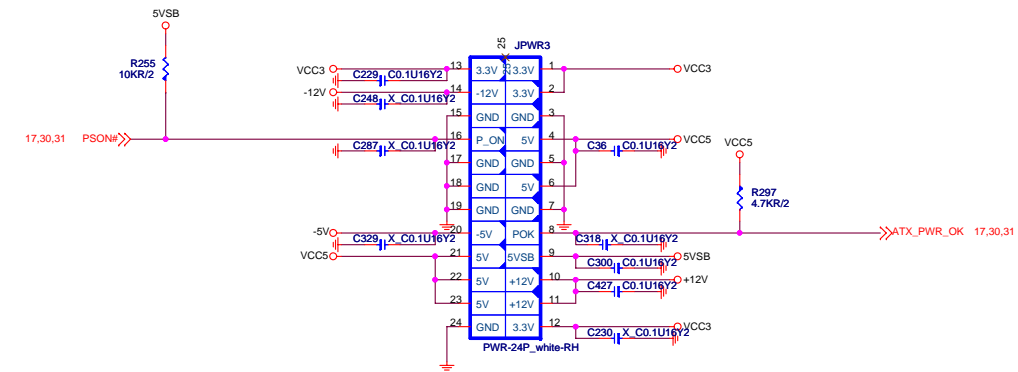
ISL6334 4Phase



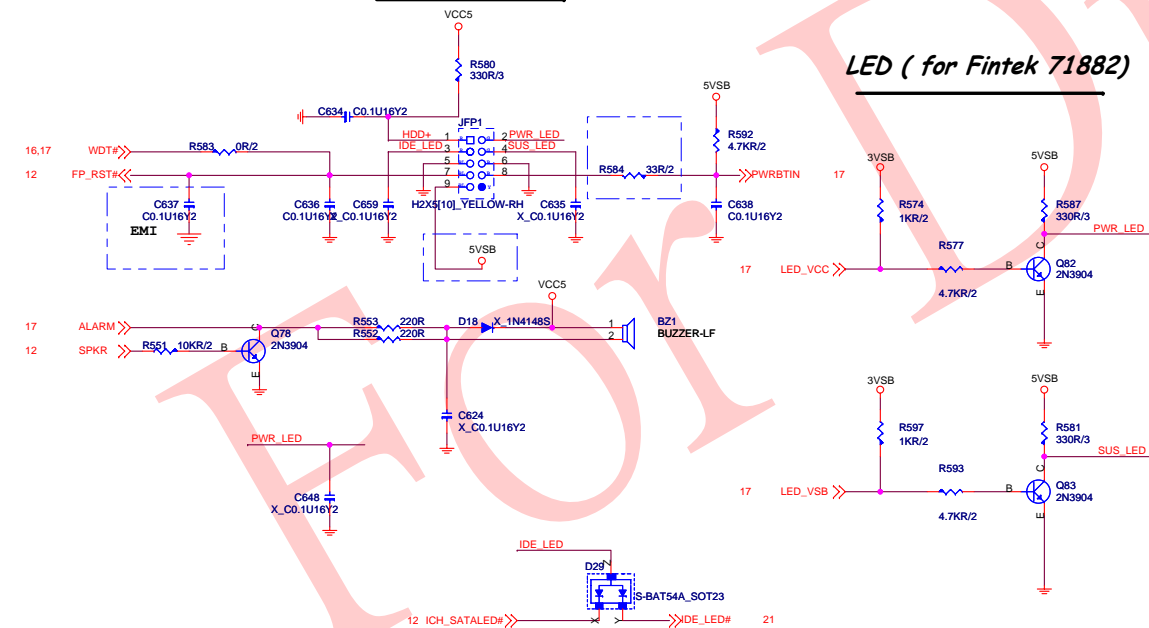
PSI (POWER STATE INDICATOR)



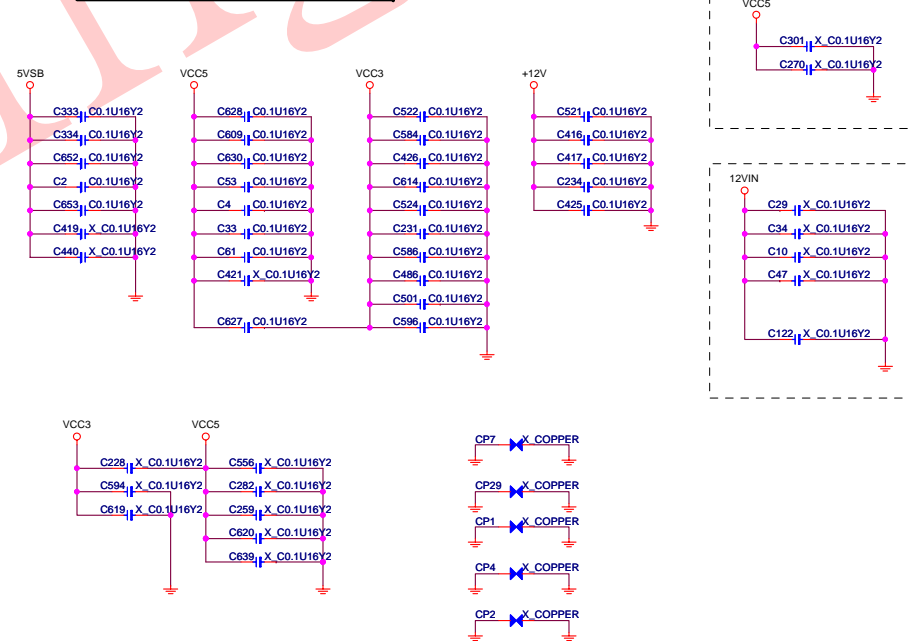
ATX POWER CONNECTOR



FRONT PANNEL



Cap. for EMI & Power

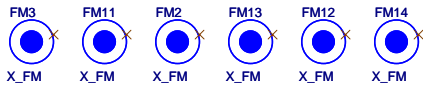


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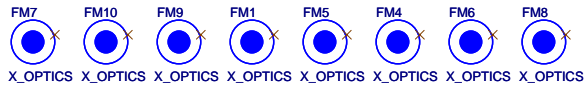
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Size	Document Description	Rev
Custom	ATX PWR-Connector & Front Panel	0A
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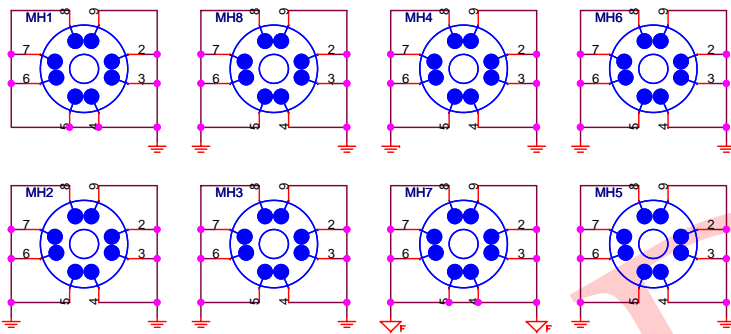
Optical Fiducial Marks-120



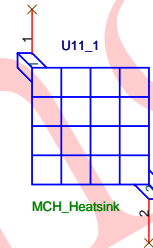
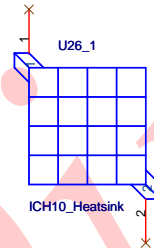
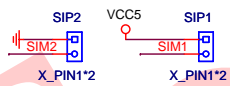
Optical Fiducial Marks-100



Mounting Holes



Simulation



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Size B	Document Description Manual Parts & Option Parts	Rev 0A
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Ver.	Change List	Page
0B	1. VRM Modify	
	Change R12,16,26,32 =>6.98Kohm ,C16 =>15pF	30
	R22=>300ohm,R39=>2.49Kohm,R43=>20Kohm	
	Stuff EC3 EC9	
	2. Power team recommend	
	change C79=>10nF, EC31=>1000uF	
	replace Q32,34=>D03-0480600-O05	29
	change C328=>10nF,EC33,34 =>remove,EC37,39=>470uF,EC32,35,36=>820uF	
	ADD EC110 =>820uF	
	replace Q43=>D03-0903BDB-N03,Q42,73=>D03-75N022B-N03	29
	3. Add Q72,R362 NB power switch circuit turn off NB power	29
	4. follow demo circuit Add R870 Stuff for NON-Intel LAN	12
	5. For DVI stuff R717,R718,R719, change RN79,RN80 => 22R	24
	6. R133=>1.58K,R295=>10.7K for DDR, NB power margin	29
	7. For customer requests change R909,R910=> 0603	13
	8. Change R92=> 1k for chip_power_good level	28
	9. Improve V_1P5_ICH VR's MOS temperature	28
	remove R326,C383,R320,R608,C379,EC100.R374,Q47	
	stuff EC41	
	replace Q52 => D03-75N022B-N03 ,U18=> I71-LM35833-B28	
	10. VRM Modify Improve temperature	
	replace Q2,Q3,Q7,Q9,Q10,Q14,Q15,Q17=> D03-75N022B-N03	30
	11. Add EC33 for V_FSB_VTT	28
	12. For INTEL Design Review	
	Change C740 =>0.1u	08
	Add C980,C981,C982,C983 =>0.1u	
	for VREF_CA_A,VREF_CA_B,VREF_DQ_A,VREF_DQ_B	14,15
	Near SB ball U1 Add C984,C985 =>0.022u	13
	Near SB ball AC9 Add C986 =>0.1u	13
	For VccGLAN1_5 change C445=>4.7u/X5R ,C443=>2.2u/X5R	13
	For 5VREF ,5VREF_SUS change C571 ,C611=>1uF/X7R	13
	For VccRTC near the ball A22 C505 => 1uF/Y5V	13
	For V_1P05_VCCAUX Add C987=>0.1uF/X7R ,C561 => 1uF/Y5V	13
	For VCCA_EXP	
	remove L29 , Add R915=>1Ω ,L39 = 600 Ω (FB) ,C612=> 1uF	09
	For VCCA_DAC	
	Add L39 = 600 Ω (FB) , change R892 =>1Ω ,	09
	For VCCDQ_CRT	
	Add L40 = 600 Ω (FB) , change R702 =>1Ω ,C613=>1u	09
	C613 will be 1u for onbroad graphic	
	BOM Option will be 0 ohm for no onbroad graphic	
	For FSB_VTT require	
	Add C988 C989 C990=> 2.2uF	09
	For VCC_Core require backside caps 10uF x(3/4) and 1uF x(6/8)	09
	C300,C562,C767=> 10uF	
	change C307 C323 C382 C416 C884 C975 C977 C371 =>1u	
	VCC_Core require caps 22uF x3, 1uF x3 and 10uF x3	09
	Add C991,C992.C993 => 22uF Add C763 C765 C762 =>10uF	
	change C976 C302 C311 =>1uF	
	VCC_EXP require caps 2.2uF x3	09
	Add C994,C995.C996 => 22uF	
	VCCSM require caps 2.2uF x6	09
	change C262=2.2uF , ,Add C263,C264,C269,C268,C267 =>2.2uF	

Ver.	Change List	Page
0B	For SRTCST# Required	12
	change R456 => 20KΩ and C513=>1uF	
	For NB1.AR2 Required	09
	change R706 Empty R709 stuff	
	13. Reserve R578 Q47 R478 & Add R802 for Plug - in issue	30
	14. For INTEL Design Review change C262 to 2.2uF Add C250	09
	15. Change VGA DVI to new VGA DVI (N58-39F0031-SK7)	18,24
	16. COM1 change to JCOM1	17
	17. Add R872 & R873 for NB&DDR power layout	29
	18. Add U56,C997,C998,C999 ,EC108 for KB/MS power circuit	17
	19. change SVCC1,SVCC2 to SVCC_Real	26
	change SVCC3,SVCC4 ,SVCC4 to SVCC_Front	27
	change SVCC6 to SVCC_MCR	
	SWAP JUSBF & JUSBMRC	27
	20. ADD C674,C675C677,C680 For EMI	31
	21. change R780,R778,R777,R776 for audio Precision	22
	22. Reserve for Plug - in issue SWAP Q47 D,S	30
	23 Change Vaule Empty or Stuff state In Shm circuit For P45 + ICH10 SKU	
	24 follow intel demo Design change R227 to 150R	29
	25 No-stuff R514, Stuff R505 with 10Kohm	12
	1 Disable PSI# patch circuit.	
	Empty (-)R242,R253,R273,R247,C235,Q53 ,Q65 Stuff R652	
	2 DDR3 Power Correction.	
	Change R133 1.58K1% to 1.5K1%	
	3 Beep sound	
	Empty R75	
	4 Replace USB connector.	
	N53-08M0171-K06 ==> N53-08M0191-F02	
	5 Remove HDA Function.	
	Empty (-)R860,R861,R862,R863,R864,R865,R866,R867,R859 ,JHDA1	
	6 LAN USB connector	
	Empty	
	7 SIO related Issues.	
	Empty (-)R789 (+)R112	



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